

Date of deposit

nsmitted herewith for filing is the Patent Application of:

Tyentor: CHI-CHUN CHEN, TZU-LIANG LEE, SHIH-CHANG CHEN

## METHOD OF FORMING DUAL GATE INSULATOR LAYERS FOR CMOS APPLICATIONS

Enclosed are:						U.S. PTC	
x	2 sheets of drawing(s) - formal.						
$\begin{bmatrix} x \end{bmatrix}$	An assignment of the invention to Taiwan Semicondutor Manufacturing Co.						
	An assignment of the invention to Taiwan Semicondutor Manufacturing Co.  An associate power of attorney Applicant claims small entity status						
	Request & Ce	& Certification under 35 USC 122(b)(2)(b)(i)					
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BASIO	C FEE	><	> <		\$ 750.		
ТОТА	L CLAIMS	33 -20=	13	x 18 =	\$ 234.		
	P CLAIMS	<b>2</b> -3=	0	x 84 =	\$ 0.		
				SUB TOTAL	\$ 984.		
				ASSIGNMENT	\$40.		
				TOTAL	\$ 1.024.		
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I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed to Assistant Commissioner of Patents, Alexandria, VA, 22313-1450. Applicant and/or Attorney requests the date of deposit as the Filing Date.

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